In re Patent Application of:
RAYNOR ET AL.
Serial No. **09/993,387**
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In the Specification:

Please replace the paragraph beginning at page 6, lines 8-18, with the following rewritten paragraph:

The operation of the array is as follows. At point 1 (see Figure 7) the [[RST]] Rst signal goes high, causing all the M2 transistors (M2_1, M2_2, etc.) to conduct and the voltage [[Vpix]] Vplx on the photodiode to be reset to [[Vrt]] VRt. At a time later point 2 (see Figure 7), all the S1 switches (S1_1, S1_2, etc.) are closed simultaneously and the output of the sense transistors (M1) are stored on the sense capacitors (Csn_1, Csn_2). Subsequently (not shown), the signals on the sense capacitors are readout sequentially by sequentially closing switches S2 (S2_1, S2_2, etc.).